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gAPZ0092
E-band Power Amplifier
81-86 GHz (76-90 GHz)

FEATURES

- 81-86 GHz
- 28/30 dBm P1dB/PSAT
- 35 dBm OIP3
- 19 dB gain
- Integrated detectors
- Nominal bias: 4.0 V and 1.3 A
- Size: 4 x 2.5 x 0.05 mm

APPLICATIONS

- Point-to-point communication
- Radar and imaging
- Instrumentation
- Fiber over radio

DESCRIPTION

The gAPZ0092A is a bare die GaAs pHEMT four-stage power amplifier MMIC optimized for 81-86 GHz. It has 19 dB gain and 35 dBm OIP3 making it ideal for long-range spectral efficient E-band point-to-point communication.

At a nominal bias of 4.0 V and 1.3 A the MMIC dissipates 5.2 W and deliver 30 dBm saturated power at 15 % PAE.

Two temperature compensated detectors are integrated on-chip and can be configured for RMS power or envelope detection.

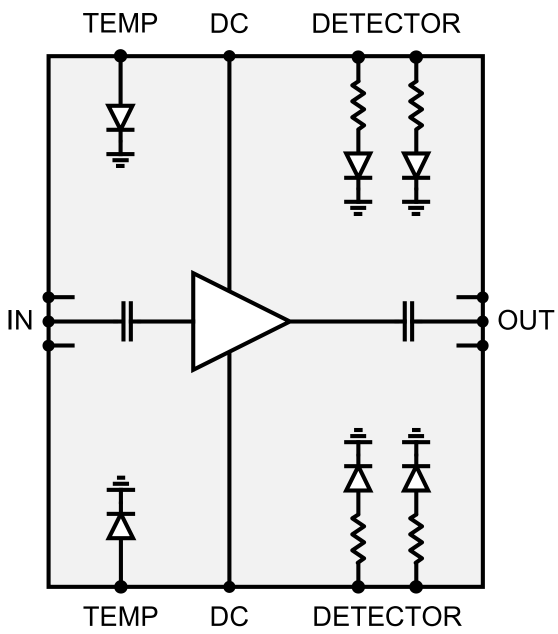

Figure 1. Circuit block diagram

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ELECTRICAL SPECIFICATIONS

Table 1. Electrical specifications, backside temperature +25 °C, nominal bias

Parameter		**Min**	**Typ**	**Max**	**Unit**
Frequency Range (performance)		81		86	GHz
Frequency Range (extended)		76		90	GHz
Gain			19		dB
Gain Temperature Slope			-0.05		dB/°C
OP1dB			28		dBm
PSAT (3 dB compression)			30		dBm
PAE at PSAT			15		%
OIP3			35		dBm
Input Return Loss			15		dB
Output Return Loss			15		dB
Detector Output at POUT *(VREF - VDET)*	-10 dBm		3		mV
	0 dBm		20		
	10 dBm		100		
	20 dBm		500		
	30 dBm		2000		
PDC (quiescent)	3.3 V / 1.3 A		4300		mW
	4.0 V / 1.3 A		5200		

Table 2. Absolute maximum ratings

Gate voltage (VG..)	-2.0 V
Drain voltage (VD..)	+4.5 V
Drain currents:	
VD1_A or VD1_B (one-sided bias)	360 mA
VD1_A and VD1_B (two-sided bias)	400 mA
VD2_A or VD2_B (one-sided bias)	480 mA
VD2_A and VD2_B (two-sided bias)	520 mA
VD3_A or VD3_B (one-sided bias)	720 mA
VD3_A and VD3_B (two-sided bias)	800 mA
RF input power	+20 dBm
Junction temperature (1 million hours MTTF) *Thermal resistance (+85 °C backside temp, incl. epoxy)*	+150 °C *9 °C/W*
Operating temperature	-40 to +85 °C
Storage temperature	-65 to +150 °C

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Pad Configuration and Bias

Always apply the gate supplies first followed by the drain supplies. It is recommended to initially set all gates to -1.6 V and adjust the gate supplies to obtain the specified drain currents.

The typical gate voltage can vary by up to 0.2 V from what is noted. The drain currents are listed with all RF input signals off.

When gates and drains are combined external to the chip using a common gate and drain supply, adjust the common gate voltage to achieve a total drain current of 1.3 A.

Table 3. Pad configuration on connector P1

Pad No.	Reference	Supply (V)	Current (mA)	Function
1	TEMP	See temperature sensor		Temperature output
2	VG1_A	-0.5 (typ.)		Bias
3	VD1_A	4.0	150	Bias
4	VG2_A	-0.5 (typ.)		Bias
5	VD2_A	4.0	200	Bias
6	GND			GND
7	VG3_A	-0.5 (typ.)		Bias
8	VD3_A	4.0	300	Bias
9	VREF_A	See detector operation		Detector reference
10	VDET_A			Detector output

Table 4. Pad configuration on connector P2

Pad No.	Reference	Interface	Function
11	GND		GND
12	RF_OUT	50 Ohm, open-circuit at DC	RF output
13	GND		GND

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Table 5. Pad configuration on connector P3

Pad No.	Reference	Supply (V)	Current (mA)	Function
14	VDET_B	See detector operation		Detector output
15	VREF_B			Detector reference
16	VD3_B	4.0	300	Bias
17	VG3_B	-0.5 (typ.)		Bias
18	GND			GND
19	VD2_B	4.0	200	Bias
20	VG2_B	-0.5 (typ.)		Bias
21	VD1_B	4.0	150	Bias
22	VG1_B	-0.5 (typ.)		Bias
23	TEMP	See temperature sensor		Temperature output

Table 6. Pad configuration on connector P4

Pad No.	Reference	Interface	Function
24	GND		GND
25	RF_IN	50 Ohm, open-circuit at DC	RF input
26	GND		GND

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Typical Performance

Unless otherwise noted, all data presented has been obtained from on-wafer measurements, at room temperature and at nominal bias.

The two-tone RF input signal at -8 dBm/tone has a separation frequency of 50 MHz.

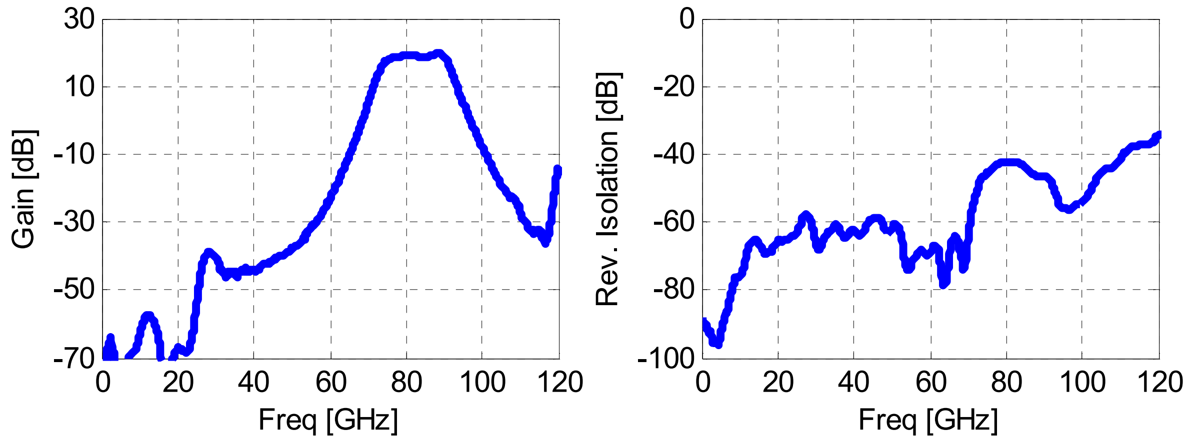

Figure 2. Gain (left) and reverse isolation (right)

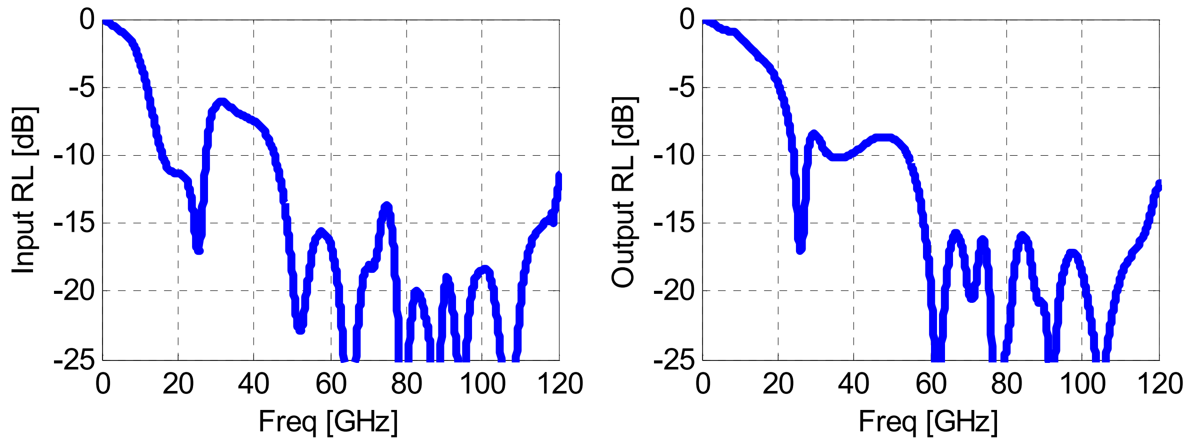

Figure 3. Input (left) and output return loss (right)

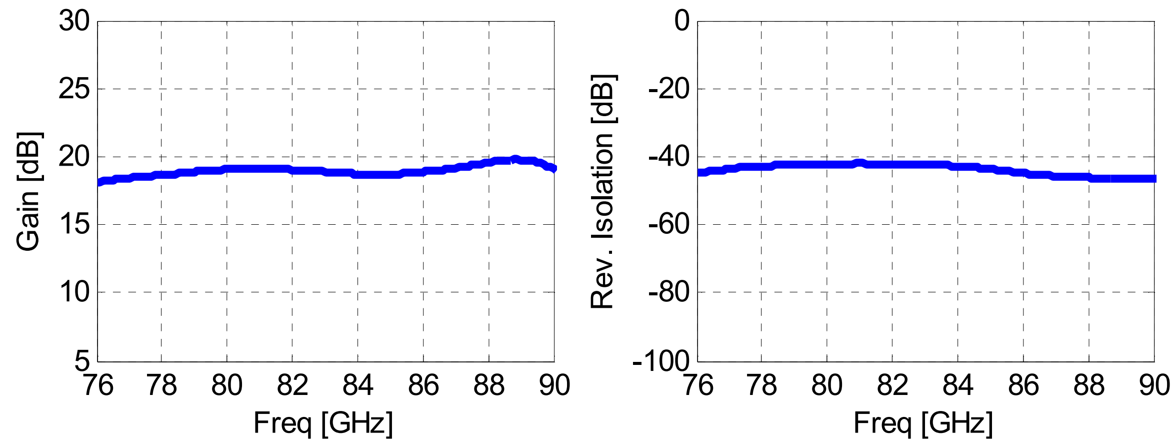

Figure 4. In-band gain (left) and reverse isolation (right)

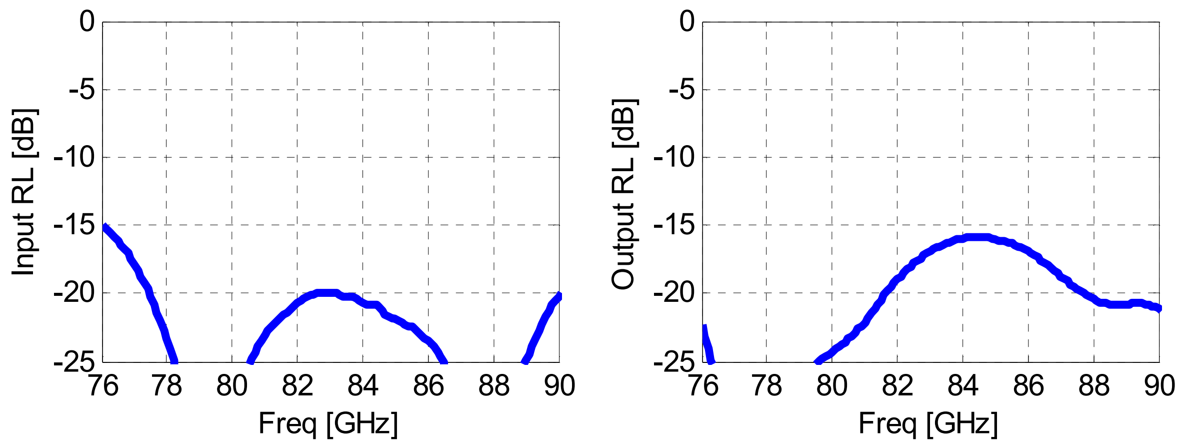

Figure 5. In-band input (left) and output return loss (right)

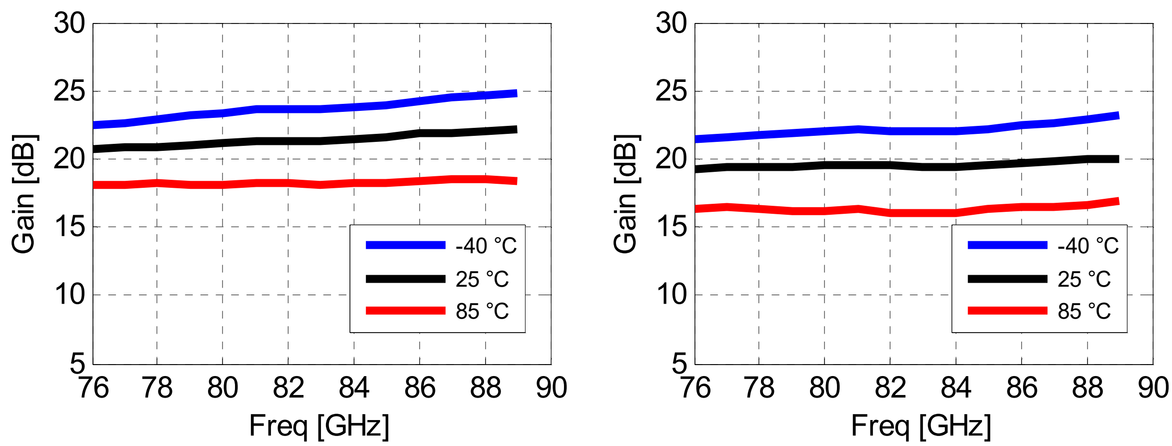

Figure 6. Gain at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

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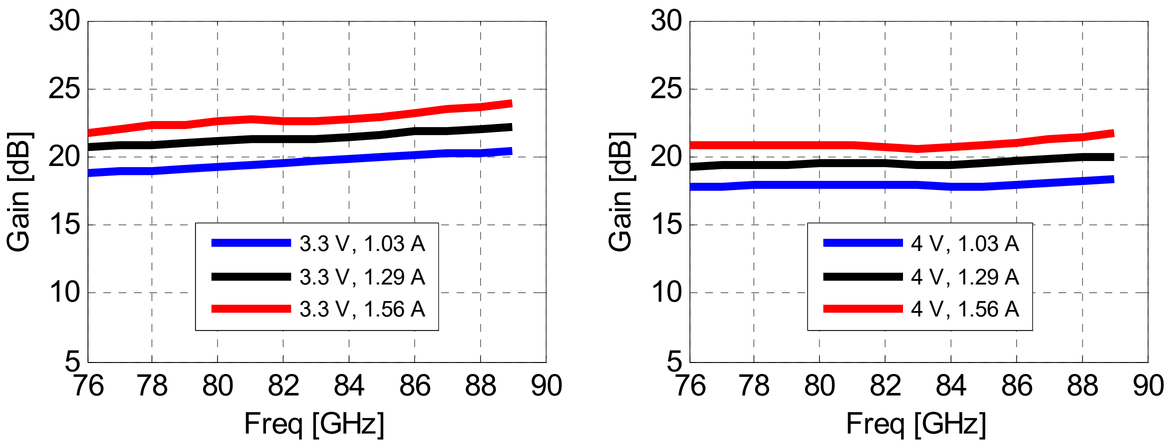

Figure 7. Gain at 3.3 V (left) and 4.0 V (right)

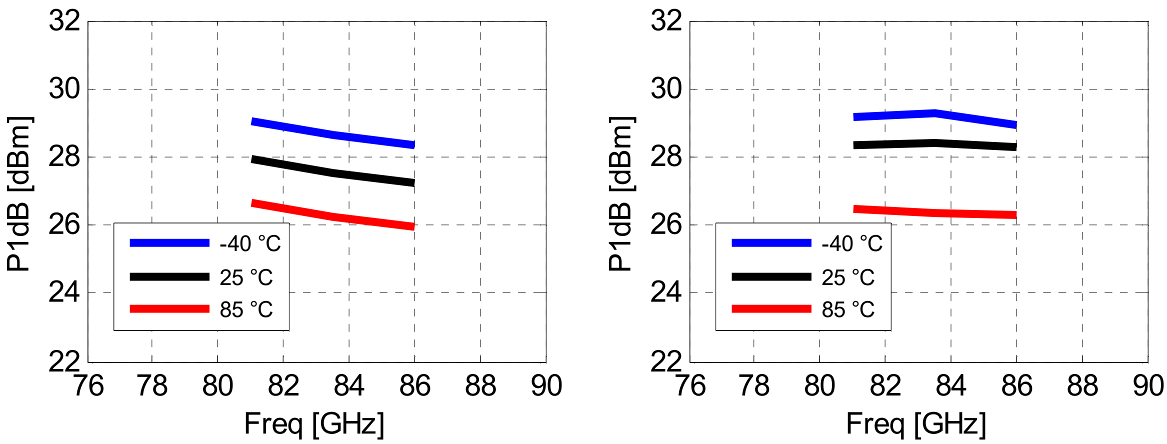

Figure 8. P1dB at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

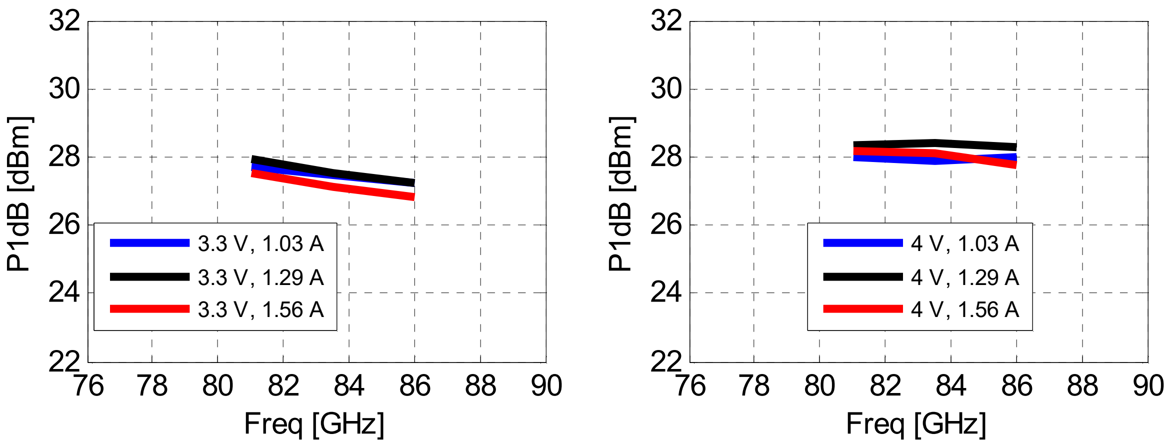

Figure 9. P1dB at 3.3 V (left) and 4.0 V (right)

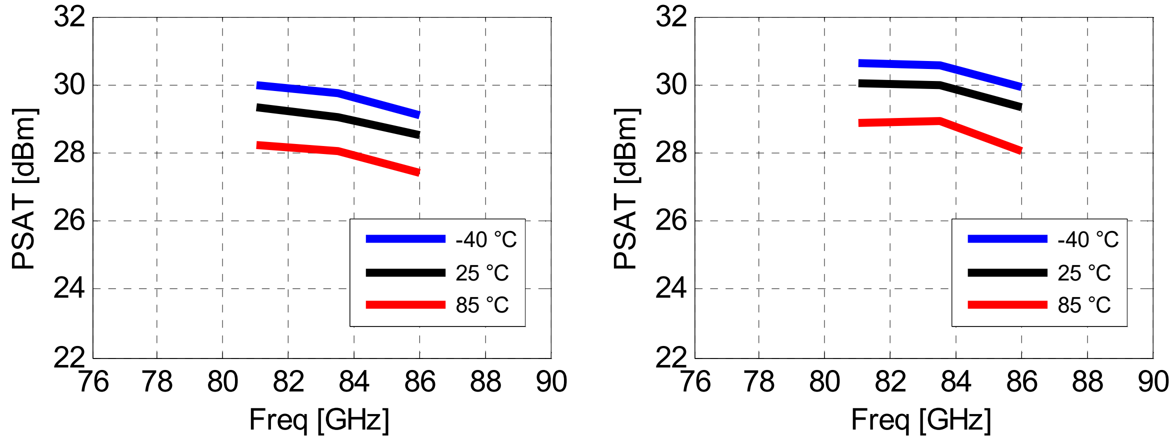

Figure 10. PSAT at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

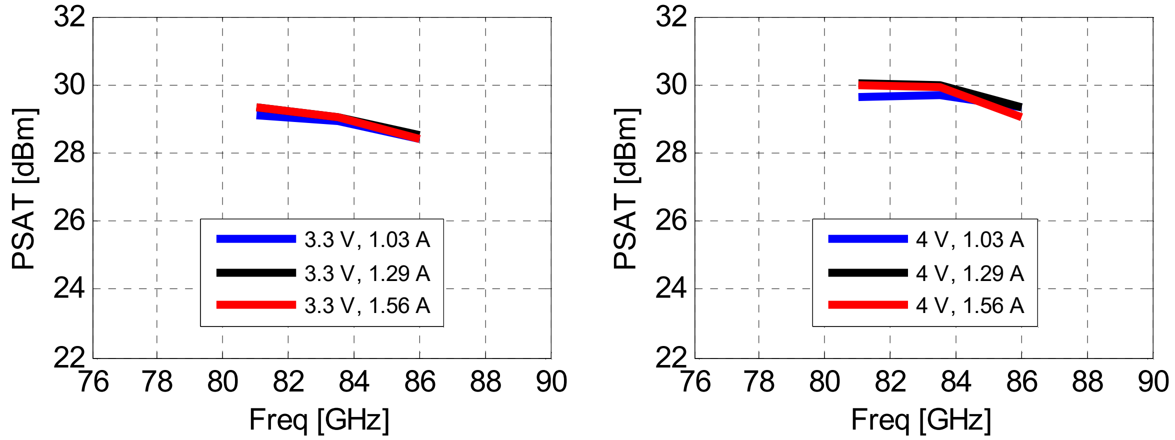

Figure 11. PSAT at 3.3 V (left) and 4.0 V (right)

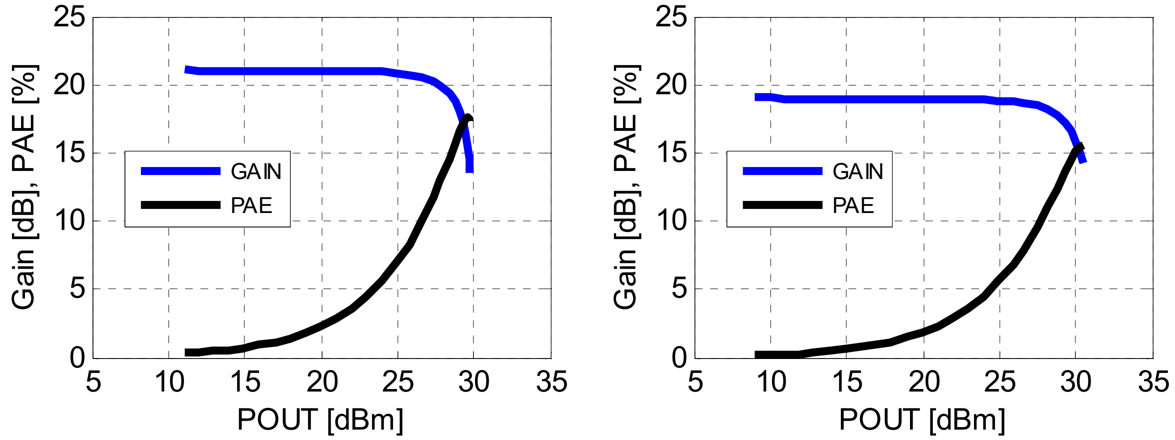

Figure 12. PAE at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right), 83.5 GHz

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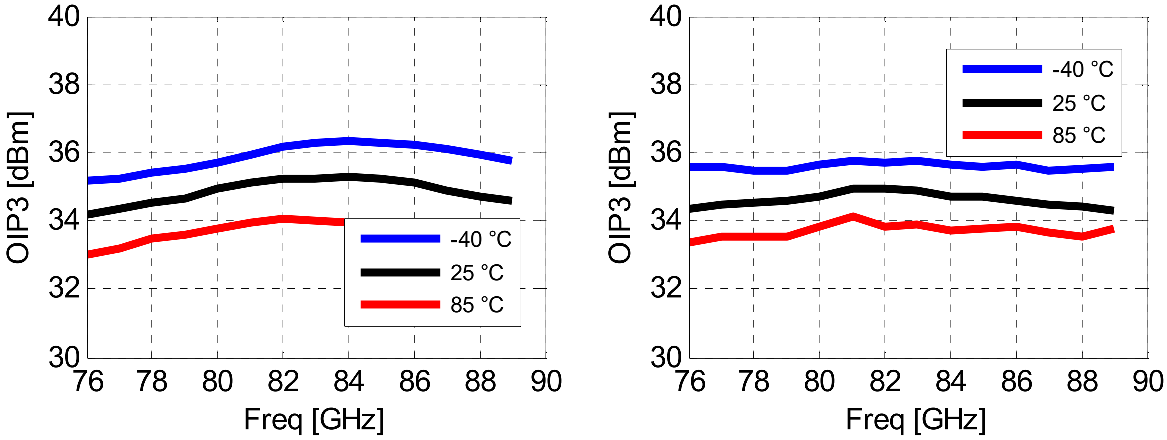

Figure 13. OIP3 at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right)

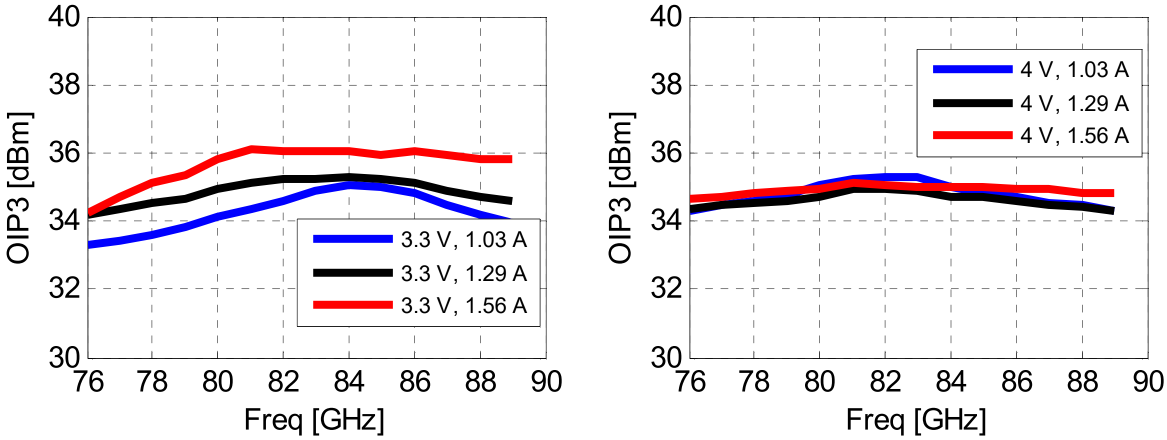

Figure 14. OIP3 at 3.3 V (left) and 4.0 V (right)

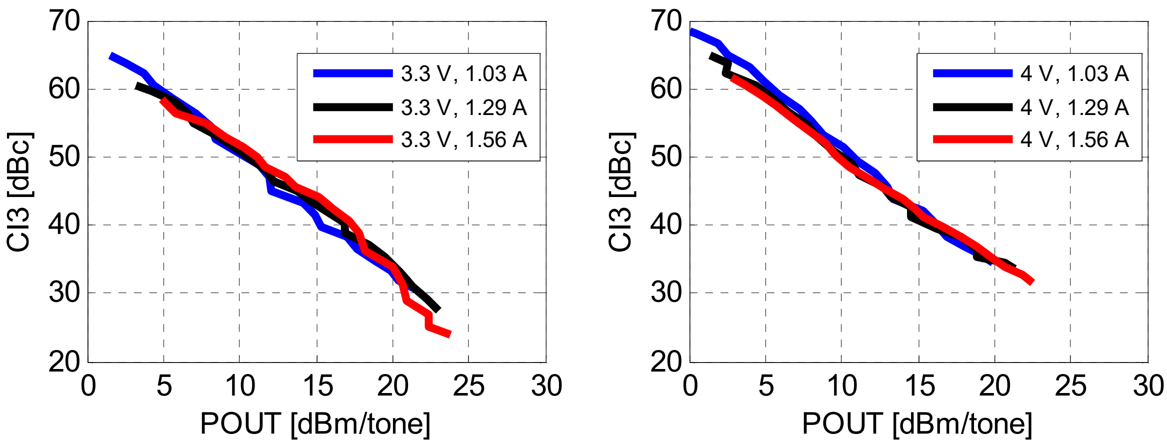

Figure 15. CI3 at 3.3 V (left) and 4.0 V (right), 83.5 GHz

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Detector Operation

There are two identical detectors on-chip, detector A and B. Each detector can be configured for RMS power or envelope detection. Leave VREF and VDET as no-connect if not used.

To compensate for thermal variation, a reference is included on chip. Therefore, to get a temperature compensated output, take the difference of VREF and VDET using the recommended external detector circuit. Detector bias is applied through VDD and a pair of resistors (R1 and R2), ideally with close to identical values, typically 10k to 100k. We recommend selecting an operational amplifier with excellent input offset voltage performance, eg. LT1012.

Envelope Detection

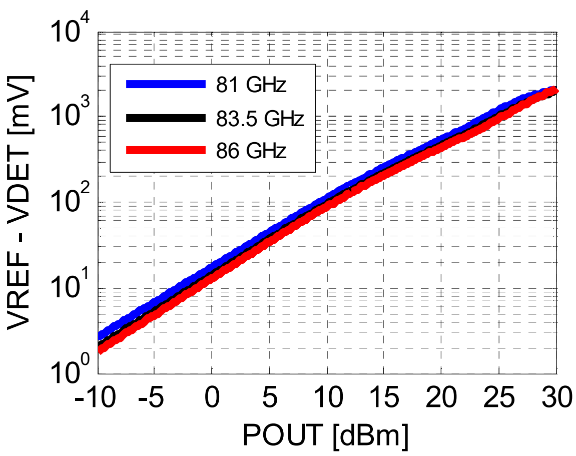
When configured for envelope detection it is necessary to keep transmission-line lengths to a minimum and select external components with good RF performance to support wide bandwidth baseband signals.

With a bias-T, which can be as simple as a shunt resistor and a series capacitor connected to VDET, the bias current is regulated with the resistor while the envelope signal can pass the capacitor. Typical bias current is 1 mA.

Input impedance at the pad of VDET is 200 Ohm. The reference output, VREF, is not required for envelope detection.

Temperature Sensor

A PN-diode temperature sensor with grounded cathode is available on-chip. Typical bias current is 100 uA and can be achieved by connecting eg. a 36.5k resistor between TEMP and a +5.0 V supply. Diode voltage is 1210 mV (typ.) at +25 °C and -1.4 mV/°C.



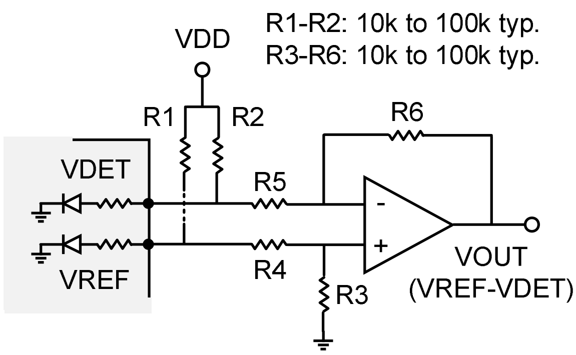


Figure 16. Detector output (left) and the external detector circuit (right)

Assembly Diagram

Gates and drains on side A are connected on-chip to the corresponding gates and drains on side B. The die can be powered by connecting supplies to drains on A, B or both sides and similarly the same applies for gates. Always make sure that the rated maximum drain current is never exceeded. For high-power applications we therefore recommend connecting drain supplies to both A and B.

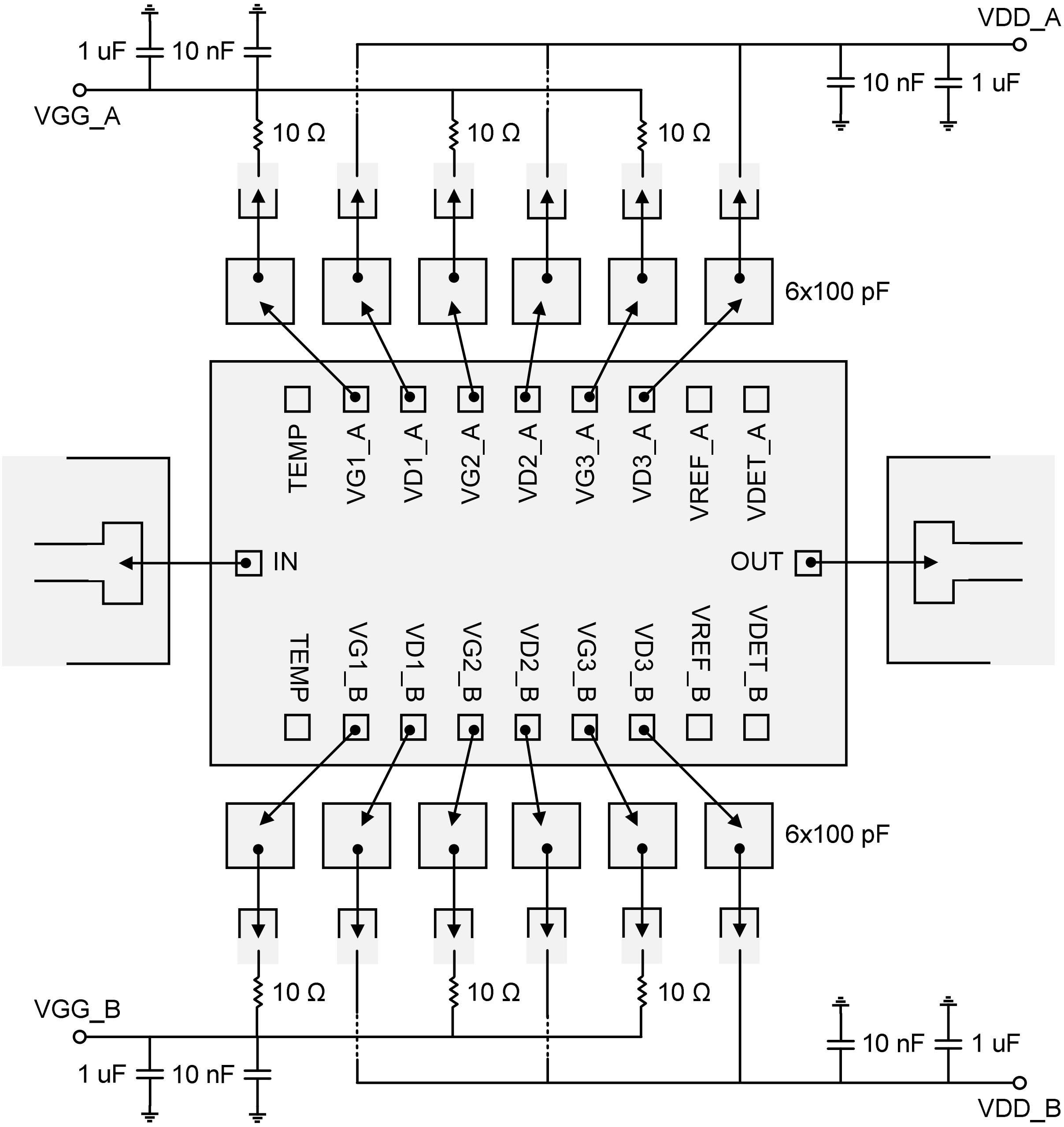


Figure 17. Assembly diagram

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Assembly Guidelines

Mount the die to an electrically grounded plane with excellent thermal properties. Make sure the surface is clean and flat before attaching the die. Both solder and epoxy can be used, we recommend eg. CM 124-08 silver epoxy.

Bonding

The input and output is pre-matched to 50 Ohm at the pad. For optimum performance keep bond-wires as short as possible and apply an external bond-wire inductance matching network. Bonding outside the area of a pad may damage the passivation layer.

DC Bypass

For stable operation locate external DC bypass capacitors near the die to reduce the bond-wire length and corresponding inductance. See assembly diagram for a recommended bypass network. Use high quality SLCs, eg. CSM-200-10X10X5-G-101-Y and low ESR ceramic or tantalum SMD capacitors.

Outline Drawing

Dimensions are in um. The MMIC thickness is 50 um. A dxf file is also available on request for use with CAD tools.

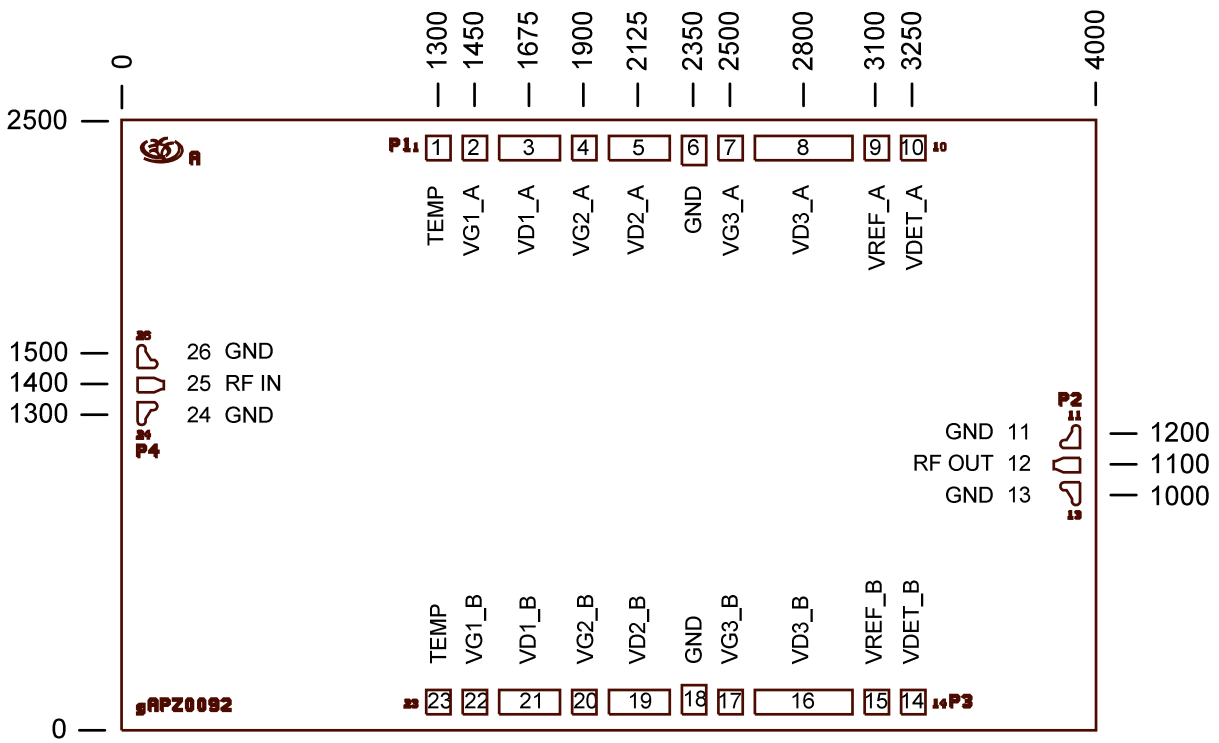

Figure 18. MMIC outline drawing

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